METHOD OF MANUFACTURING
FLASH MEMORY DEVICE

BACKGROUND

Field of the Invention

[0001] The present invention relates to a method of manufacturing a flash memory device, and more particularly to a method of manufacturing a flash memory device capable of reducing a difference in effective field oxide heights ("EFH") between a high voltage transistor area, and a low voltage transistor/cell area, which is caused by respective protruding portions of element isolation films thereon in a flash memory device manufactured by applying a self-align shallow trench isolation ("SA-STI") scheme.

Discussion of Related Art

[0002] Basically, a flash memory device has low voltage transistors and high voltage transistors in order to drive cells according to necessary properties. Usually, a gate oxide film for the high voltage transistor is made to be thick, on the other hand, in case of the low voltage transistor, it is made to be thin. The thickness of a gate oxide film for a cell is equal or similar to that for a low voltage transistor. The steps caused by a difference in thickness of the gate oxide films between the high voltage transistor area and the low voltage transistor/cell area result in different thickness of the nitride films which remain after the subsequent chemical mechanical polishing for forming the element isolation films in each of areas. Also, this generates a difference in EFH's between the high voltage transistor area and the low voltage transistor/cell area. Herein, the EFH means a difference in heights of the element isolation films based on the contact surface of a first poly-silicon layer for a floating gate and a second poly-silicon layer for a floating gate.

[0003] Shown in Fig. 1 is a cross-sectional view illustrating a conventional method of manufacturing a flash memory device formed by applying a self-align shallow trench isolation scheme. Although a flash memory device includes a cell area, a low voltage transistor area, and a high voltage transistor area, the cell area and the low voltage transistor area will be

considered as one area - the low voltage transistor/cell area - in the following descriptions for easier understanding because the thickness of their gate oxides is similar to each other.

[0004] Referring to Fig. 1, a gate oxide film 12A for a high voltage is formed on a semiconductor substrate 11 in a high voltage transistor area HV, and another gate oxide film 12B for a low voltage/cell is formed on a semiconductor substrate 11 in a low voltage transistor/cell area LV/CELL. The gate oxide film 12A in a high voltage transistor area HV is thicker than the gate oxide film 12B in a low voltage transistor/cell area LV/CELL. A first poly-silicon layer 13 for a floating gate is formed on the gate oxide films 12A and 12B. A plurality of isolation trenches are formed on the semiconductor substrate 11 by performing an SA-STI process. Thereafter, element isolation films 160 are formed by filling isolation oxide materials into the trenches 15. A second poly-silicon layer 19 for a floating gate is formed on the whole surface of the structure, including the element isolation films 160. Although it is not shown in the drawing, gates are formed on respective areas by performing an etching process using a mask for a floating gate, a process of forming a dielectric film, a process of forming a conductive layer for a control gate, and an etching process using a mask for a control gate.

[0005] According to the conventional method of manufacturing a flash memory device described above, each of protruding portions of element isolation films 160 in the high voltage transistor area HV and the low voltage/cell area LV/CELL causes a difference in EFH's between these areas. Generally, the effective field oxide height EFH1 based on the first poly-silicon layer 13 in the high voltage transistor area HV becomes (-) 50 to 100 Å, whereas the effective field oxide height EFH2 based on the first poly-silicon layer 13 in the low voltage transistor/cell area LV/CELL becomes in the range of 300 Å to 800 Å. The effective field oxide height EFH2 in the low voltage transistor/cell area LV/CELL has a higher and wider range of values. Furthermore, the values become different depending on the processing conditions of a chemical mechanical polishing. Such a difference in EFH's between the high voltage transistor area HV and the low voltage transistor/cell area LV/CELL and the high value of EFH's in the low voltage transistor/cell area LV/CELL, causes some problems such as difficulties in establishing a gate etching target for each area, bad pattern profiles of the gate, and reasons of failures caused by the poly-silicon remnants. Since these problems become important as devices are highly integrated, continuous efforts have been made to solve them.

SUMMARY OF THE INVENTION

[0006] Accordingly, the present invention is directed to provide a method of manufacturing a flash memory device capable of reducing a difference in effective field oxide heights between a high voltage transistor area and a low voltage transistor/cell area, which is

caused by respective protruding portions of element isolation films thereon so as to ensure process safety and improve device reliability.

[0007] According to the present invention, a method of manufacturing a flash memory device includes providing a semiconductor substrate having a high voltage transistor area in which a first gate oxide film and a first poly-silicon layer are formed between first element isolation films, and a low voltage transistor/cell area in which a second gate oxide film and the first poly-silicon layer are formed between second element isolation film. The method also includes forming a planarizing film on the surfaces of the first poly-silicon layer and the first and second element isolation films, removing upper portions of the planarizing film and the element isolation films in the low voltage transistor/cell area to a certain thickness by performing a first etching process, and removing upper portions of the planarizing film and the element isolation films in the high voltage transistor area and the low voltage transistor/cell area by performing a second etching process. The method also includes forming a second poly-silicon layer on surfaces of the first poly-silicon layer and the element isolation films.

[0008] In addition, the first and second etching processes are performed by a wet etching process using an oxide etching solution with HF added.

[0009] Furthermore, the first and second etching processes can be performed to obtain effective field oxide heights in the high voltage transistor area and the low voltage transistor/cell area of about (-) 100 to about 50 Å.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The aforementioned aspects and other features of the present invention will be explained in the following description, taken in conjunction with the accompanying drawings, wherein:

[0011] Fig. 1 is a cross-sectional view illustrating a conventional method of manufacturing a flash memory device; and,

[0012] Figs. 2A to 2F are cross-sectional views illustrating a method of manufacturing a flash memory device according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0013] The present invention will be described in detail by way of the preferred embodiment with reference to the accompanying drawings, in which like reference numerals are used to identify the same or similar parts.

[0014] Shown in Figs. 2A to 2F are cross-sectional views for illustrating a method of manufacturing a flash memory device formed by applying a SA-STI scheme according to an embodiment of the present invention.

[0015] Although a flash memory device includes a cell area, a low voltage transistor area, and a high voltage transistor area - the cell area and the low voltage transistor area will be considered as one area - the low voltage transistor/cell area - in the following description for easier understanding because the thickness of their gate oxides is similar to each other.

[0016] Referring to Fig. 2A, a gate oxide film 22A for a high voltage is formed on a semiconductor substrate 21 in the high voltage transistor area HV, and a gate oxide film 22B for a low voltage/cell is formed on the semiconductor substrate 21 in the low voltage transistor/cell area LV/CELL. The gate oxide film 22A in the high voltage transistor area HV is formed to be thicker than the gate oxide film 22B in the low voltage transistor/cell area LV/CELL. A first poly-silicon layer 23 for a floating gate is formed on the gate oxide films 22A and 22B. A plurality of isolation trenches are formed on the semiconductor substrate 21 in the high voltage transistor area HV and the low voltage transistor/cell area LV/CELL by forming a nitride film 24 on the first poly-silicon layer 23 and then performing an etching process using an SA-STI scheme for the nitride film 24, the first poly-silicon layer 23, the gate oxide film 22A and 22B, and the semiconductor substrate 21. An oxide film for element isolation 26 is formed to cover the whole structure, including the isolation trenches 25 so as to sufficiently fill the trenches 25. The oxide film for element isolation 26 is usually made of a material having an excellent gap filling capability and a high insulating characteristic, such as an HDP oxide.

[0017] Referring to Fig. 2B, a chemical mechanical polishing process is performed to form element isolation films 260 in the trenches 25 just until the surface of the first poly-silicon layer 23 in the high voltage transistor area HV is exposed. As recognized in the drawing, there is a difference in the heights of the remaining nitride film 24 and the protruding portions of the element isolation films 260 based on the surface of the first poly-silicon layer 23 between the high voltage transistor area HV and the low voltage transistor/cell area. As described above in the conventional method, the EFH's of the element isolation films 260 in the high voltage transistor area HV are smaller than those in the low voltage transistor/cell area LV/CELL so that there is a difference between both areas. This causes the problems as described above in the conventional method.

[0018] Referring to Fig. 2C, the remaining nitride films 24 are removed. Then, a buffer oxide film 27 is formed to cover the surfaces of the first poly-silicon layer 23 and the element isolation films 260 having different heights. Also, a planarizing film 28 is formed on the buffer oxide film 27.

[0019] In the above description, the buffer oxide film 27 has a thickness of about 100 Å or less, preferably about 20 to about 100 Å, in order to prevent contamination that may occur when the planarizing film 28 directly contacts the first poly-silicon layer 23. Also, the buffer oxide film 27 is not required but, preferable is present to prevent the contamination. The planarizing film 28 is made of a material that has high fluidity and excellent planarization, such as a spin on glass (SOG) or a boron phosphorous silicate glass (BPSG) having a thickness in the range of about 300 Å to about 800 Å.

[0020] Referring to Fig. 2D, a photo resist pattern 30 is formed on the planarizing film 28 to open the low voltage transistor/cell area LV/CELL and close the high voltage transistor area HV. The planarizing film 28 and the element isolation films in the low voltage transistor/cell area LV/CELL are removed to a certain thickness by an etching process using a photo resist pattern 30 as an etching mask.

[0021] In the above description, a wet etching may be performed by using an oxide etching solution with HF added. Under the same etching condition, the etching rate of a planarizing film 28 formed by an SOG or a BPSG is faster than that of an element isolation film 260 formed by an HDP. By such etching processes, the upper portions of the element isolation films 260 in the low voltage transistor/cell area LV/CELL are partially removed to reduce the EFH's.

[0022] Referring to Fig. 2E, the photo resist pattern 30 is removed. Then, the planarizing film 28, the buffer oxide film 27, and the element isolation films 260 in the high voltage transistor area HV and the low voltage transistor/cell area LV/CELL are removed by a blanket etching process.

[0023] In the above description, the photo resist pattern 30 is removed by a wet or dry method. The blanket etching process is performed by a wet etching using an oxide etching solution with HF added until the first poly-silicon layer 23 is exposed. Under the same etching conditions, the etching rate of the planarizing film 28 formed by an SOG or a BPSG is faster than that of the element isolation film 260 formed by an HDP. By such etching processes, the upper portions of the element isolation films 260 in the high voltage transistor area HV as well as the low voltage transistor/cell area LV/CELL are partially removed to reduce the EFH's of the element isolation films 260 in each of areas HV and LV/CELL. As a result, the EFH's of the element isolation films 260 in the high voltage transistor area HV and the low voltage transistor/cell area LV/CELL are about (-) 100 to about 50 Å. Therefore, it is possible to remarkably reduce the difference in the EFH's between the both areas HV and LV/CELL. Meanwhile, if a wet etching is used to remove the photo resist pattern 30, it is possible to perform the etching process that uses a photo resist pattern 30 as an etching mask shown in Fig. 2D, the process of removing the photo resist pattern shown in Fig. 2E,

and the blanket etching process shown in Fig. 2E in the same machine in a sequential manner.

[0024] Referring to Fig. 2F, the surfaces of the element isolation films 260 and the first poly-silicon layer 23 are planarized on the whole area, HV and LV/CELL, without any step. Then, the second poly-silicon layer 29 for a floating gate is formed on the planarized surface. Although it is not shown in the drawings, gates are formed in each area by performing the subsequent processes, such as an etching process using a mask for a floating gate, a process of forming a dielectric film, a process of forming a conduction layer for a control gate, and an etching process using a mask for a control gate.

[0025] As described above, according to the present invention, it is possible to reduce a difference in effective field oxide heights between a high voltage transistor area and a low voltage transistor/cell area, which is caused by respective protruding portions of element isolation films thereon, thus ensuring process safety and improving device reliability.

[0026] Although the foregoing description has been made with reference to the preferred embodiments, it is to be understood that changes and modifications of the present invention may be made by the ordinary skilled in the art without departing from the spirit and scope of the present invention and appended claims.